CLAIMS

We claim:

1. In a system of finite state machines built with synchronous logic for controlling the flow of data through computational logic circuits programmed to accomplish a task specified by a user, having one finite state machine associated with each computational logic circuit, having each finite state machine accept data from either one or more predecessor finite state machines or from one or more sources outside the system and furnish data to one or more successor finite state machines or a recipient outside the system, excluding from consideration in determining a clock period for the system logic paths performing the task specified by the user, and providing a means for ensuring that each finite state machine allows sufficient time to elapse after the computational logic circuit associated with that finite state machine has obtained input data that all signals generated within such computational logic circuit in response to such input data have propagated through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic circuit.

2. The system as recited in claim 1, wherein:

the means for ensuring that each finite state machine allows sufficient time to elapse after the computational logic circuit associated with that finite state machine has obtained input data that all signals generated within such computational logic circuit in response to such input data have propagated through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic circuit is a count-down timer wherein a register is set to a sufficient number of clock cycles for the computational logic circuitry to perform its task and decremented with each clock until reaching zero.

3. The system as recited in claim 1, wherein:

the means for ensuring that each finite state machine allows sufficient time to elapse after the computational logic circuit associated with that finite state machine has obtained input data that all signals generated within such computational logic circuit in response to such input data have propagated through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic

circuit is a count-up timer wherein a register is set to zero and increased with each clock until reaching a sufficient number of clock cycles for the computational logic circuitry to perform its task.

4. The system as recited in claim 1, wherein:

the means for ensuring that each finite state machine allows sufficient time to elapse after the computational logic circuit associated with that finite state machine has obtained input data that all signals generated within such computational logic circuit in response to such input data have propagated through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic circuit is configuring each finite state machine with sufficient wait states for all signals generated within such computational logic circuit in response to such input data to propagate through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic circuit.

5. In a system of finite state machines built with asynchronous logic for controlling the flow of data through computational logic circuits programmed to accomplish a task specified by a user, having one finite state machine associated with each computational logic circuit, having each finite state machine accept data from either one or more predecessor finite state machines or from one or more sources outside the system and furnish data to one or more successor finite state machines or a recipient outside the system, excluding from consideration in determining a clock period for the system logic paths performing the task specified by the user, and providing a means for ensuring that each finite state machine allows sufficient time to elapse after the computational logic circuit associated with that finite state machine has obtained input data that all signals generated within such computational logic circuit in response to such input data have propagated through such computational logic circuit before communication is permitted to occur from such computational logic circuit to a subsequent computational logic circuit.